B. AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory shared by a plurality of heterogeneous processors, comprising:

the shared memory;

wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set; ~~and~~

wherein the shared memory is accessible by one or more second processors that are adapted to process a second instruction set; and

wherein the shared memory, the first processors, and the second processors are included on one silicon substrate and are connected using an on chip coherent multi-processor bus.

2. (Original) The shared memory as described in claim 1 further comprising:

a memory map corresponding to the shared memory, wherein the memory map is shared between the first processors and the second processors.

3. (Original) The shared memory as described in claim 2 further comprising:

an operating system that operates on one of the first processors, the first processor controlling the memory map.

4. (Original) The shared memory as described in claim 1 wherein each second processor further comprises:

a synergistic processing unit;

a local storage; and

a memory management unit, the memory management unit including a direct memory access controller.

5. (Original) The shared memory as described in claim 4 wherein at least one of the second processors use the direct memory access controller to access the shared memory.

6. (Original) The shared memory as described in claim 4 wherein the local storage is divided into a private storage and a non-private storage.

7. (Original) The shared memory as described in claim 6 wherein the non-private storage is included in the shared memory.

8. (Currently Amended) The shared memory as described on claim [[1]] 2 wherein the memory map includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region.

9. (Canceled)

10. (Canceled)

11. (Currently Amended) A method for sharing a memory between a plurality of heterogeneous processors, said method comprising:

receiving a memory request;

allocating a first memory partition on the shared memory that corresponds to the memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set; ~~and~~

assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set;

managing the first memory partition and the second memory partition using a common memory map; and

wherein the common memory map includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region.

12. (Canceled)

13. (Currently Amended) The method as described in claim [[12]] 11 wherein one of the first processors includes an operating system whereby the first processor controls the common memory map.

14. (Canceled)

15. (Original) The method as described in claim 11 wherein at least one of the first processors is a Power PC and wherein at least one of the second processors is included in a synergistic processing unit.

16. (Original) The method as described in claim 15 wherein the shared memory corresponds to the synergistic processing unit.

17. (Original) The method as described in claim 11 wherein at least one of the second processors uses a direct memory access controller for accessing the shared memory.

18. (Currently Amended) A computer program product stored on a computer operable media for sharing a memory between a plurality of heterogeneous processors, said computer program product comprising:

means for allocating a first memory partition on the shared memory that corresponds to the memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set; ~~and~~

means for assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set; and

means for managing the first memory partition and the second memory partition using a common memory map that includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region.

19. (Canceled)

20. (Currently Amended) The computer program product as described in claim [[19]] 18 wherein one of the first

processors includes an operating system whereby the first processor controls the common memory map.

21. (Canceled)

22. (Original) The computer program product as described in claim 18 wherein at least one of the first processors is a Power PC and wherein at least one of the second processors is included in a synergistic processing unit.

23. (Original) The computer program product as described in claim 22 wherein the shared memory corresponds to the synergistic processing unit.

24. (Original) The computer program product as described in claim 18 wherein at least one of the second processors uses a direct memory access controller for accessing the shared memory.

25. (Currently Amended) A memory shared by a plurality of heterogeneous processors, comprising:

the memory, wherein the memory includes one or more non-private storage areas, the non-private storage areas included in ~~corresponding to~~ one or more second processors that are adapted to process a second instruction set and access the memory; and

wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set and access the memory.

26. (Original) The shared memory as described in claim 25 wherein each second processor further comprises:

synergistic processing logic which uses private storage, the private storage not included in the shared memory; and

memory management logic for directly accessing the shared memory.

27. (Original) The shared memory as described in claim 25 further comprising:

memory mapping logic that corresponds to the shared memory, wherein the memory mapping logic is shared between the first processors and the second processors.

28. (Original) The shared memory as described in claim 27 further comprising:

an operating system that operates on one of the first processors, the first processor controlling the memory mapping logic.

29. (Original) The shared memory as described in claim 25 wherein one of the first processors configures each of the non-private storage areas.